EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S107	620	(logic near design) and (layout near design) and @ad<"20031128"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/07 20:08
S108	230	(logic near design) and ((layout physical) near design) and (@ad< '20031128" and ((allocat\$5 floorplan\$5 ((floor ad) plan\$5) insert\$3) with (clock\$3 clk delay buffer driver repeater))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/07 20:17
S109	18	@ad<"20031128" and (optim\$7 verif\$7 correct\$3 fix\$4) near5 (timing time clock\$3 delay skew) with ((before prior\$2 preced\$4) near3 (layout))	US-PGPUB; USPAT; USOOR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/07 20:26
S113	2523	@ad<"20031128" and delay and skew and ((logic circuit functional (front near2 end)) with (phase stage designs3 process\$3 routine)) and ((physical layout (back near2 end)) with (phase stage design \$3 process\$5 routine))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 01:39
S115	421	@ad<"20031128" and delay and skew and ((logic circuit functional (front near2 end)) with (phase stage design\$\$ process\$\$ routine)) and ((physical layout (back near2 end)) with (phase stage design \$\$ process\$\$ routine)) and ((number value) with (clock tree buffer driver repeater)) and (sta or ((time timing transient spice) near3 (analv\$\$7)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 01:42

S114	1856	@ad<"20031128" and delay and skew and ((logic circuit functional (front near2 end)) with (phase stage design\$3 process\$3 routine)) and ((physical layout (back near2 end)) with (phase stage design \$3 process\$5 routine)) and ((number value) with (clock tree buffer driver repeater))	US-POPUB; USPAT; USOOR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 01:42
S116	421	@ed<"20031128" and delay and skew and ((logic circuit functional (front add 2 end)) with (phase stage design\$3 process\$3 routine)) and ((physical layout (back add 2 end)) with (phase stage design \$3 process\$3 routine)) and ((number value) with (clock tree buffer driver repeater)) and (sta or ((time timing transient spice) near3 (analy\$7)))	US-PAPUB; USPAT; USCOR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 01:43
S117	230	@ad<"20031128" and delay and skew and ((logic circuit functional (front add 2 end)) with (phase stage design\$ process\$3 routine)) and ((physical layout (back add 2 end)) with (phase stage design \$3 process\$3 routine)) and ((number value) with (clock tree buffer driver repeater)) and (sta or ((time timing transient spice) near3 (analy\$7)) and (sta (clock near3 arree) (allocat\$4 near4 (clock clk buffer driver)' (clock clk buffer driver)' (clock clk tree) near2 build\$3))	US-PGPUB; USPAT; USOOR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 01:45
S118	76	@ad<"20031128" and delay and skew and ((logic circuit functional (front add 2 end)) with (phase stage design\$ process\$3 routine)) and ((physical layout (back add 2 end)) with (phase stage design \$3 process\$3 routine)) and ((number value) with (clock tree buffer driver repeater)) and (sta or ((time timing transient))	US-PCPUB; USPAT; USCOR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 01:46

		spice) near3 (analy\$7))) and (cts (clock near3 tree) (allocat\$4 near4 (clock dib buffer driver)) ((clock clk tree) near2 build\$3)) and "716" clas.		***************************************	***************************************	***************************************
S119	2701	@ad<"20031128" and (timing netilist sta (logic near (design phase stage))) with (verif\$7 optim \$7 test\$3 check\$4 fix\$4 correct\$5) and (layout with (verif\$5 optim\$7 test\$3 check\$4 fix\$4 correct\$5))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 14:17
8120	238	@adc "20031128" And ((technology near lond) independent) (front adj end) functional rtl hdl ((gate near level) near (specification description)) nellist (logicS near 2 (phase stage design\$3 process\$3 routine)) with ((timing near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3)) sta spice) And ((technology near dependent) (back adj end) layout (physical near2 (phase stage design\$3 process\$3 routine))) with ((timing near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3)) sta spice) And (clock timing buffer) with (spec specification configuration requirement definition defin\$3)	USPAT; USOA; EPO; JPO; DEFWENT; IBM_TDB	OR	ON	2010/04/08
S121	206	@ad-"20031128" And (1echnology near independent) (front adj end) functional rtl hdl ((gate near level) near (specification description)) nellist (logis2 near2 (phase stage design\$3 process\$3 routine))) with ((timing near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3)) sta spice) And ((technology near dependent) (back adj end) layout (physical near2 (phase stage design\$3	US-PG-PUB; US-PG- US-OR; EPO; JPO; DEF-WENT; IBM_TDB	OR	ON	2010/04/08 14:24

		process\$3 routine)) with (timing near5 (ana)\\$5 closure converg\\$5 verif\\$5 optim\\$7 chec\\$4 static validat\\$3)) sta spice) And (clock timing buffer) with (spec specification configuration requirement definition defin\\$3) and \"716" clas.		***************************************	annennennennennennennennennennennen	
S122	161	@ad-"20031128" And ((technology near independent) (front adj end) functional rth hdl ((gate near level) near (specification description)) netlist (logic\$2 near2 (phase stage design\$3 process\$3 routine)) with ((timing near5 (analy\$5 closure converg\$5 verif\$5 closure converg\$6 verif\$6 clock timing buffer) with (spec specification definition definitio	(US-PGP-UE; USPAT; USCOR; EPO; JPO; DETWENT; IBM_TDB	OR	ON	2010/04/08
S123	1	@ad<"20031128" And (netilist near5 ((gate near level) rtl functional logic \$2) with (!timing near5 (analy\$5 closure converg \$5 verif\$5 optim\$7 check \$4 static validat\$3)) sta spice) And (!time timing timed) near3 (driv\$3)) near3 layout)	US-PCPUB; USPAT; USOCR; EFO; JPO; DERWENT; IBM_TDB	OR	NO.	2010/04/08 14:47

\$126	4233	@ad< "20031128" And ((netlist near5 ((gate near level) rlt verilog vhd functional logic\$2) (gate adj level) (logic\$2 adj (stage phase design routine)) ((dock buffer) with (skeleton synthesis tree))) with ((timing near5 (analy\$5 dosure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3)) sta spice)) And (layout same ((timing near5 (analy\$5 dosure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3 driven based)) sta spice)) And Delay And Skew\$3 And (dock timing puffer) with (spec specification configuration requirement definition defin \$3 character\$7 constraint goal) or (identify\$7 determin\$5 calculat\$4 ascertain\$5) with (dock near (net source domain structure element block near she she with (allocat \$4 defin\$5 generat\$5 distribut\$3 allot\$5 appropriat\$3 earmark\$3 apportion\$3 saign\$5)	US-PCPUB; USPAT; USCOR; FPRS; EPO; JPO; DEFWENT; IBM_TDB	OR	ON	2010/04/08 16:06
S127	72	@ad<"20031128" And (netilst (((gate ad) level) netilst (1 (d) verilog vhdl logic\$2) adj (stage phase design routine)) ((dock buffer) near4 (skeleton synthesis ree)) ((dock buffer) near2 (tree distribution) near2 synthes \$7) with ((timing near5 (analy\$5 closure converg\$5 optim\$7 check \$4 static validat\$3)) sta spice)) And [layout same ((timing near5 (analy\$5 closure converg\$5 verif\$5 closure converg\$5 verif\$5 closure converg\$5 verif\$5 closure converg\$5 verif\$5 closure distribution) and bleay And Skew\$3 And ((dock timing buffer) with (spec specification configuration requirement definition defin \$3 character\$7 constraint	US-PGPUB; USPAT; USCOR; FPRS; EPC; JPC; DEFWENT; IBM_TDB	OR	ON	2010/04/08

S129	575	apprropriat\$3 earmark\$3 apportion\$3 asign\$5] ((dook buffer) near2 (tree distribution) near2 (synthes \$7))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 16:25
55128	72	earmarks3 apportions3 asign\$5) @ad<"20031128" And (netlist ((gate ad) level) netlist (1 flut verilog vhdl logic\$2) ad] (stage phase design routine)) ((dock buffer) near4 (skeleton synthesis tree)) ((dock buffer) near2 (tree distribution) near2 (stree sistribution) near2 (synthes \$7 build\$3 produc\$4 generat\$4 creat\$4))) with ((liming near5 (analy\$5 closure converg\$5 verit\$5 optim\$7 check\$4 static validat\$3)) sta spice)) And (layout same ((timing near5 (analy\$5 optim\$7 check\$4 static validat\$3) and (clock timing buffer) with (spec specification configuration requirement definition definis\$ character \$7 constraint goal) or ((identify\$7 determin\$5 claracter \$7 constraint goal) or ((identify\$7 determin\$5 list \$3 report\$3) with (clock near (net source domain structure element block neas*4 used utiliti\$7)) had (clock buffer) with (allocat\$4 defin\$5 generat	US-POPUB; USPAT; USOOR; FFRS; EPO; JPO; DEHWENT; IBM_TDB	OR .	ON	2010/04/08 16:22
		goal) or ((identify\$7 determin\$5 calculat\$4 ascertain\$5 list\$3 report \$3) with (clock near (net source domain structure element block need\$4 used utiliz\$7))) And (clock buffer) with (allocat\$4 defin \$5 generat\$5 distribut\$3 iallot\$5 appropriat\$3 earmark\$3 apportion\$3		***************************************		

S130	246	((dock buffer) near2 (tree distribution) near2 (synthes \$7)) and @ad<"20031128"	US-PGPUB; USPAT; USCOR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 16:31
S131	411	@ad-"20031128" And (netist (((gate adj level) netist (((gate adj level) netist it hd verilog vhdl logic\$2) adj (stage phase design routine)) sane (((timing time delay slack \$3 skew\$3 transient) near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validats\$3 simulat\$4 emulats\$5 predict \$44)) sta spice\$2) And (layout same ((timing near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validats\$3 driven based)) sta spice\$) And Delay And Skew\$3 And ((alock timing buffer) with (spec specification configuration requirement definition defin\$3 character\$7 constraint goal permission rule attribut\$4) or ((identify\$7 determin\$5 calculat\$4 ascertain\$5 list \$3 report\$3) with (clock near6 (net path source domain structure element block need\$4 used utiliz\$7 component)) And (clock buffer) with (allocas\$4 detin) this 5 generat\$5 distribut\$3 alot\$5 appropriat\$3 earmark\$3 apportion\$3 alot\$5 appropriat\$3	US-PAT-US-COR; FPRS; EPO; JPO; DEFWMENT; IBM_TDB	OR	ON	2010/04/08 16:35
S132	403	@ad-"20031128" And (netist (((gate adj level) netist (((gate adj level) netist ith di verilog vhdl logic\$2) adj (stage phase design routine)) sane (((timing time delay slack \$3 skew\$3 transient) near5 (analy\$5 dosure converg\$5 verit\$5 optim\$7 check\$4 static validat\$3 simulat\$4 emulat\$5 predict \$41) sta spice\$2)) And (layout same ((timing near5 (analy\$5 dosure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3	US-PGPUB; USPAT; USCOR; FFRS; EPC; JPC; DEBWENT; IBM_TDB	OR	ON	2010/04/08 16:38

		driven based)) sta spice) And Delay And Skew\$3 And ((dock timing buffer) near10 (spec specification configuration requirement definition defin\$3 character \$7 constraint goal permission rule attribut\$4 description) or ((identify \$7 determin\$5 calculat\$4 ascertain\$5 list\$3 report \$3) with (clock near6 (net path source domain structure element block need\$4 used utiliz\$7 component!)) And (dock buffer) with (allocat\$4 defin\$5 generat\$5 distribut\$3 allot\$5 appropriat\$3 earmark\$3 apportion\$3 asign\$5 budget\$4)				
S133	402	Ged-"20031128" And (netist ((gate adj level) (circuit adj list\$3) rtl hdi verliog vhdl logic\$2) adj (stage phase design routine))) sane ((timing time delay slack\$3 skew\$3 transient) near5 (analy\$5 closure converq\$5 verif\$5 optim\$7 check\$4 static validat\$3 simulat\$4 emulat \$5 predict\$4)) sta spice \$2)) And (layout same ((timing near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3 driven based)) sta spice)) And Delay And Skew\$3 And ((dock timing buffer) near10 (spec specification configuration requirement definition defin\$3 character \$7 constraint goal permission rule attribute description propert\$4) or ((identify\$7 determin\$5 ist \$3 report\$3) with (dock near6 (net path source domain structure element block need\$4 used utiliz\$7 component))) And (dock buffer) with (allocat\$4 define defining generat\$5 distribut\$3 allot\$5 distribut\$3 allot\$\$5 distribut\$3 allot\$5 dispredict\$4 appropriat\$5 earmark\$3	US-PAT-US-COR- US-PAT-US-COR- FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 16:43

		apportion\$3 asign\$5 budget\$4)				
5134	414	(netlist (((gate ad) level) (circuit adj list\$3) rll hdl verilog vhdl logic\$2) adj ((stage phase design routine)) sane ((timing time delay slack\$3 skew\$3 transient) near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$5 smulat\$4 emulat\$5 predict\$4)) sta spice \$2) And (layout same ((timing near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3 driven based simulat\$4 emulat\$5 predict\$4)) sta spice \$2) And Clayout same ((timing near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3 driven based simulat\$4 emulat\$5 predict\$4)) sta spice) And Delay And Skew\$3 And ((lock timing buffer) near10 (spec specification configuration requirement definition defin\$3 character \$7 constraint goal permission rule attribute description propert\$4) or ((identify\$7 determin\$5 calculat\$4 ascertain\$5 list \$3 report\$3) with (clock near6 (net path source domain structure element block need\$4 used utiliz\$7 component)) And (clock buffer) with (allocat\$4 define defining generat\$5 distribut\$3 alot\$5 appropriat\$3 earmark\$3 apportion\$3 asign\$5 budget\$4)	US-PGPUB; USPAT; USOOR; FPRS; EPO; JPO; DEFWENT; IBM_TDB	OR	ON	2010/04/08
5135	6752	out\$3) ((place\$1 placing placement) near2 (route routing routed))) or ((dock buffer) near4	US-PATUR; US-PAT; US-COR; FFFRS; EPO; JPO; DEFEWENT; IBM_TDB	OR	ON	2010/04/08

S136	1033249	(((timing time delay slack \$3 skew\$3 transient) near5 (analy\$5 closure converg\$5 verif\$7 optim\$7 check\$4 static validat\$3 simulat\$4 emulat\$5 predict \$4 evaluat\$3)) sta spice \$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 18:17
S137	172	@adc "20031128" And ((((((net schematic (gate add evel) rtl) add list\$3) netlist\$3) (((gate add level) (circuit add list\$3) rtl indl verilog vhdl logic\$2) add (cycle stage phase design routine description synthes\$7 specification)) same (((timing time delay slack\$3 skew\$3 transient) near\$ (analy\$5 closure converg\$5 verif\$7 optim\$7 check\$4 static validat\$3 simulat\$4 emulat\$5 predict\$4 evaluat\$3) sta spice\$5!) And (((layout ((lay\$3 laid) add out\$3) ((lace\$1 placing placement) near\$ (route routing routed)) or ((dock buffer) near\$ (tree distribution) near\$ (synthes\$7 build\$3 produc\$4 generat\$4 creat\$4)) same ((timing near\$ (analy \$5 closure converg\$5 verif\$7 optim\$7 check\$4 static validat\$3 driven based simulat\$4 emulat\$5 predict\$4 evaluat\$4 static validat\$3 driven based simulat\$4 emulat\$5 predict\$4 evaluat\$4 friends produc\$4 evaluat\$5 predict\$4 evaluat\$5 predict\$4 evaluat\$5 predict\$6 evaluat\$4 emulat\$5 predict\$6 evaluat\$5 predict\$6 evaluat\$6 predict\$6 evaluat\$6 predict\$6 evaluat\$6 predict\$6 evaluat\$6 predict\$6 evaluat\$6 evaluat\$6 predict\$6 evaluat\$6 evaluat\$7 check\$6 static validat\$6 evaluat\$7 check\$6 static validat\$6 evaluat\$7 check\$7 evaluat\$6 evaluat\$7 check\$7 evaluat\$6	US-PAT-US-OOR; FPRS, EPO; JPO; DEHWENT; IBM_TDB	OR	ON	2010/04/08
S138	141	\$137 And (layout or (lay adj out)) And ((timing near5 (analy\$5 closure converg\$5 verif\$7 optim\$7 check\$4 static validat\$3 simulat\$4 emulat\$5 predict \$4 evaluat\$3) sta spice) And ((dock timing buffer) near10 (spec specification configuration requirement definition defin\$3 character \$7 constraint goal permission rule attribute description propert\$4 ((synthesis near (soript report))) or ((extract\$3	US-PGPUB; USPAT; USOOR; FFPS; EPO; JPO; DEFWMENT; IBM_TDB	OR .	ON	2010/04/08 18:23

		identify\$7 determin\$5 identify\$7 determin\$5 ist \$3 report\$3 specify\$3 (synthesis near (soript report))) with ((dock\$3 clk buffer\$3) near6 (net path source domain structure element block need\$4 used utiliz\$7 component)) And (dock buffer) with (allocat\$4 define defining generat\$5 distribut\$3 allot\$5 appropriat\$3 earmark\$3 apportion\$3 asign\$5 budget\$4 specify\$)				
S141	68	i@adc "20031128" and (layout (post adj layout)) with ((timing near5 (analy \$5 closure converg\$5 verif 57 optim\$7 check\$4 validat \$3)) sta spice) and ((correct\$3 optim\$7 refin \$3 refinement resolv\$3 fix \$3 adjust\$4 chang\$4 revis \$3 amend\$4 rectif\$7 redress\$3 remed\$4 modif \$7 repair\$3 reshap\$3 compensat\$3 enhanc\$5 reduc\$5 alter\$5 alteratos alteratos reconstruct\$3 improv\$5 dro reparametriz\$5 debug \$5 modulat\$3 turne tuning) with (skew))	IUS-PGPUB; USPAT; USOCR; EPO; JPO; DEFWENT; IBM_TDB	OR	ON	2010/04/08 20:57
S142	110	S141 and ((correct\$3 optim \$7 refin\$3 refinement resolv\$3 in\$3 adjust\$4 chang\$4 revis\$3 amend\$4 rectif\$7 repair\$3 reshap \$3 compensat\$5 enhanc\$5 reduc\$5 alter\$3 alteration reconstruct\$3 improv\$5 dro reparametriz\$5 debug \$5 modulat\$3 tune tuning dimensioning) with delay) and ((add\$4 insert\$3 implement\$3 appenend\$3 affix\$3 boost\$4 plug\$4 supplement\$3) near4 delay with (output\$4 launch))	US-PCPUB; USPAT; USCOR; EPC; JPO; DEFWENT; IBM_TDB	OR	ÖN	2010/04/08 20:58

S143	12	S141 and ((correct\$3 optim \$7 refin\$3 refinement resolv\$3 fix\$3 adjust\$4 chang\$4 revis\$3 amend\$4 rectif\$7 redress\$3 remed \$4 modif\$7 repair\$3 reshap \$3 compensat\$3 enhanc\$5 reduc\$5 atler\$3 alteration reconstruct\$3 improv\$5 drc reparametriz\$5 debug \$5 modulat\$3 tune tuning dimensioning) with delay) and ((add\$4 insert\$3 implement\$3 appenend\$3 affix\$3 boost\$4 plug\$4 supplement\$3) near4 (delay buffer repeater) with (outout\$4 launch))	US PGPUB; USPAT; USGOR; EPC, JPO; DEFWENT; IBM_TDB	ÓR	ON	2010/04/08 20:59
S144	35		US-PCPUB; USPAT; USCOR; EPC; JPO; DEFWENT; IBM_TDB	OR	ON	2010/04/08 21:27
S146	312	(delay near2 violation)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 22:27
S147	31	@ad<"20031128" and ((dock buffer) with tree) with ((filming near5 (analy \$5 closure converg\$5 verif \$7 optim\$7 check\$4 validat \$3)) sta spice) and ((correct\$3 optim\$7 refin \$3 refinement resork\$3 fix \$3 adjust\$4 chang\$4 revis \$3 amend\$4 rectif\$7 rediress\$3 remed\$4 modif \$7 repair\$3 reshap\$3 compensat\$3 enhanc\$5 reduc\$5 alter\$3 alteration reconstruct\$3 improv\$5 drc reparametriz\$5 debug \$5 modulat\$3 tune tuning)	US-PGPUB; USPAT; USCOR; EPC; JPO; DEFWENT; IBM_TDB	ÓR	ON	2010/04/08 22:29

S149	23	@ad<"20031128" and (((clock buffer) with tree)	US-PGPUB; USPAT; USOCR;	OR	ON	2010/04/08 22:31
		or cts bct) with ((timing near5 (analy\$ closure near5 (analy\$ closure converg\$5 verit\$7 optim\$7 check\$4 validat\$3)) sta spice) and ((correct\$3 optim\$7 refine\$mst resolv\$3 fix\$3 adjust\$4 chang\$4 revis\$3 amend\$4 redit\$7 repair \$\$ reshap\$3 compensat\$3 enhand\$5 reduc\$5 alter\$3 alter\$1 alter\$1 or reconstruct\$3 improv\$5 for reparametriz \$\$ debug\$5 modulat\$3 tune tuning) with (skew)) and ((add\$4 insert\$3 aimplement\$3 appenend\$3 affix\$3 boost\$4 plug\$4 supplement\$3) near4 (delay buffer repeater)	EPO; JPO; DEFWENT; IBM_TDB			
S148	20	@ad<"20031128" and ((dock buffer) with tree) with (treiming nears (analy \$5 dosure converg\$5 verif \$7 optim\$7 refin \$3 refinement resolv\$3 fix \$3 adjust\$4 chang\$4 revis \$3 amend\$4 rectif\$7 redress\$3 remed\$4 modif \$7 repair\$3 reshap\$3 compensat\$3 enhanc\$5 reduc\$5 alteration reconstruct\$3 improv\$5 dobug\$5 modulat\$3 tune tuning) with (skew) and ((add\$4 insert\$3 implement\$3 appenend\$3 affix\$5 boost \$4 plug\$4 supplement\$3) near4 (delay buffer repeater))	US-PGPUB; USPAT; USOOR; EPC; JPO; DEFWENT; IBM_TDB	OR	ON	2010/04/08 22:31

5150	65	or cts bct) with (timing nears (analy\$5 closure converg\$5 verif\$7 optim\$7 check\$4 validat\$3)) sta spice optim\$7 and ((correct\$3 optim\$7 refix \$3 adjust\$4 chang\$4 revis \$3 amend\$4 rectif\$7 redres\$73 remed\$4 modif \$7 repair\$3 remed\$4 modif \$7 repair\$3 reshap\$3 compensat\$3 enhanc\$5 reduc\$5 alter\$3 alteration reconstruct\$3 improv\$5 dro reparametrix\$5 debug \$5 modulat\$3 tune tuning with (skew)) and ((add\$4 insert\$3 implement\$3 alpbement\$3 appenend\$3 affix\$3 boost \$4 plug\$4 supplement\$3)	US-PGPUB; USPAT; USCOR; EPO; JPO; DEFWIENT; IBM_TDB	(OR	ON	2010/04/08 22:32
		near4 (delay buffer repeater))				

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